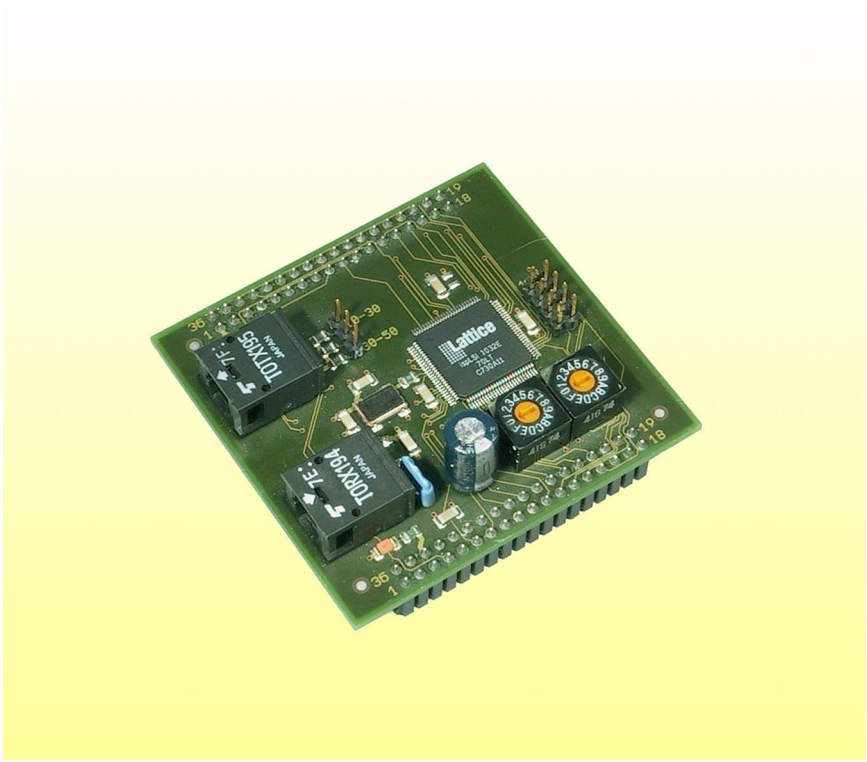
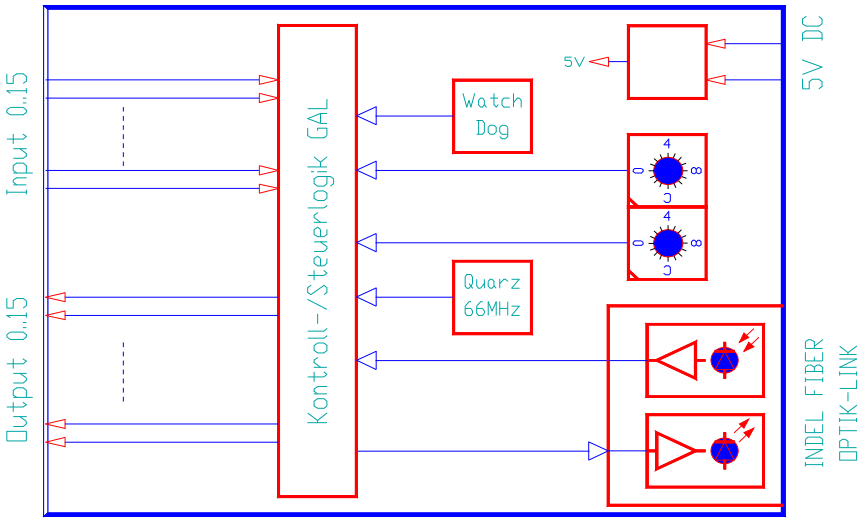
TTL-Interface

INFO-TTL



Digital INFO-Link Interface

The INFO-TTL is a universally applicable digital I/O module.
The board incorporates 16 inputs and 16 outputs with TTL level.
Two different versions are available: 1 bidirectional port with control lines, or 16 separate inputs and outputs. The module is designed for mounting on a printed circuit board. By reprogramming of the GAL logic, it is possible to incorporate additional functions; e.g. Interrupt inputs and outputs. This makes the INFO-TTL module a very flexible and cost-effective interface between existing extraneous devices and the INFO-Link.



Technical Data

Inputs
- 16 inputs
- 5V, TTL
- Maximum 4,000 inputs per INFO-Link
- Control line: Busy

Outputs
- 16 outputs
- 5V, TTL
- Maximum 4,000 outputs per INFO-Link
- Control line: Data Valid

Parallel port
- Bidirectional interface with WR, OE, CS control lines
- 16 bit data word, TTL level

Design versions
- Two different layouts: Different configuration of the INFO-Link transmitter-receiver modules.

Order-No INFO-TTL 609724201
Order-No INFO-TTL 609724201-AMK
Order-No INFO-ZLK 609724201

INDEL AG INDUSTRIELLE ELEKTRONIK

Mode of Operation

The INFO-TTL board covers 16 TTL inputs. At the same time, 16 TTL outputs can be activated.
The module can, within certain limits, be extended by additional or other functions.
The output "LED" (pin 31 on connector 2) indicates the status of the yellow LED Link Receiver Signal OK.
The following two variants have been implemented to date:

16 inputs and outputs

In the version with 16 separate inputs and outputs, the module makes two control lines available. (See Timing Diagram, page 4)

Busy signal
While the Busy signal is active (low), nothing must be written into the input register. Otherwise, invalid values may be read in.

Data Valid
The DVal signal is activated for 180ns (high) when new data is present in the output register.

Parallel port

As a parallel port, the module is addressed with the control lines WR, OE, CS. (See Timing Diagram, page 5)

IN software tems, the board behaves like an INFO-4kp. For additional infomation, see the software operating instructions in the INFO binder.

CEn	Controller Enable
QRF	Acknowledgment Enable
Syn	Start Sync Run
SyEr	Sync Position reached
NP	Zero Pulse

Connector Allocations

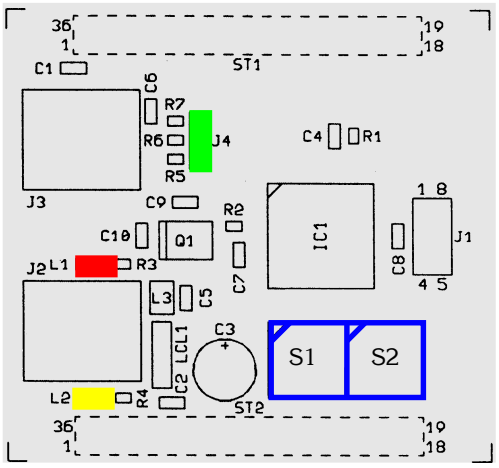
Connector 1
36 pin array
two rows

1	I	+5V		+5V	I	36
2	I	In0		WR	I	35
3	I	In1		OE	I	34
4	I	In2		CS	I	33
5	I	In3		Gnd	I	32
6	I	In4		Gnd	I	31
7	I	In5		Gnd	I	30
8	I	In6		Gnd	I	29
9	I	In7		Gnd	I	28
10	I	In8		Gnd	I	27
11	I	In9		Gnd	I	26
12	I	In10		Gnd	I	25
13	I	In11		Gnd	I	24
14	I	In12		Gnd	I	23
15	I	In13		Gnd	I	22
16	I	In14		Gnd	I	21
17	I	In15		Gnd	I	20
18	I	Gnd		Gnd	I	19

Connector 2
36 pin array
two rows

1	I	+5V		+5V	I	36
2	I	+5V		+5V	I	35
3	I	+5V		+5V	I	34
4	O	Out0		Busy	O	33
5	O	Out1		DVal	O	32
6	O	Out2		LED	O	31
7	O	Out3		CEn	O	30
8	O	Out4		QRF	I	29
9	O	Out5		Syn	O	28
10	O	Out6		SyEr	I	27
11	O	Out7		NP	I	26
12	O	Out8		Out15	O	25
13	O	Out9		Out14	O	24
14	O	Out10		Out13	O	23
15	O	Out11		Out12	O	22
16	I	Gnd		Gnd	I	21
17	I	Gnd		Gnd	I	20
18	I	Gnd		Gnd	I	19

Assembly



Addressing INFO-TTL (blau)

The INFO-TTL occupies one I/O board place (INFO-16p).

S2(0Y),S1(X0)		I/O-Karte
0	0	0
0	1	1
0	2	2
1	0	16
1	1	17
0F	0F	255

Addressing INFO-TTL AMK (blau)

The INFO-TTL-AMK occupies one channel of one INFO-4KP board.

S2(0Y),S1(X0)		4KP Karte	Kanal
0	0	0	0
0	1	0	1
0	2	0	2
0	3	0	3
1	0	1	0
1	1	1	1

LEDs on receiver module

LED-red = +5V power supply
LED-yellow = INFO-Link receiver signal OK

Transmit power jumpers (green)

The jumpers influence the illumination intensity of the emitting LED and thereby the segment length of the fiberoptic cable to the next board.

Segment length	Jumper position
0 ... 10m	no jumper
8 ... 30m	>10
20 ... 50m	>30

Specifications

Power supply

- +5V, 250mA max.
- No electrical isolation

Climatic conditions

- Ambient temperature:
  Storage: -20...+80°C
  Operation: 0 ... +45°C
- Board temperature:
  Operation: 0...+65 °C
- Relative air humidity
  no condensation: 95%

Inputs

- 16 inputs
- 5V, TTL
- No electrical isolation

Outputs

- 16 TTL outputs
- No electrical isolation

Mounting

- Printed circtuit board mounting
- Dimensions:
  63.5 x 60 x 15mm (LxWxH)

Design versions

The INFO-TTL module is available in two layout versions:
On the one hand the variant sketched above with the transmitter and receiver modules arranged one below the other, on the other hand with transmitter and receiver modules arranged opposite each other. (Receiver facing transmitter).
Please ask for the INFO-ZLK module.

Customized modifications are available as needed.

TTL-Interface

INFO-TTL 97242
INFO-ZLK 97257

The TTL-Interface uses pins 2 ... 17 (connector 1) as input signals and pins 4 ... 15, 22 ... 25 (connector 2) as output signals.

The input interface of the INFO-TTL module makes a Busy signal available.

During Busy active (low), the input word must not be changed.

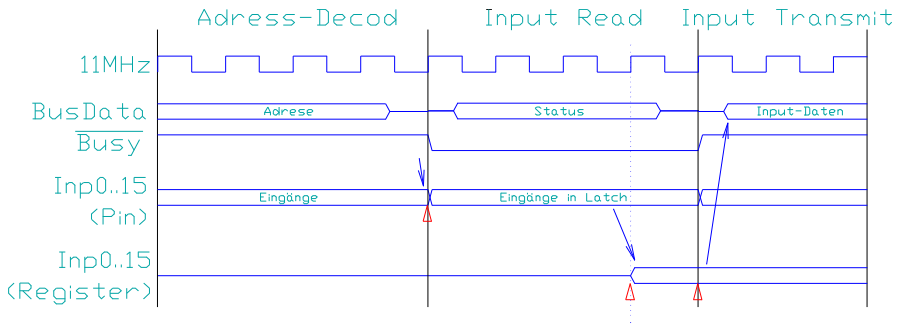
Three clock cycles after Busy active, the inputs are read in and transmitted via the bus.

The signal DVal (active high) is present during 180ns when new valid output values are present.

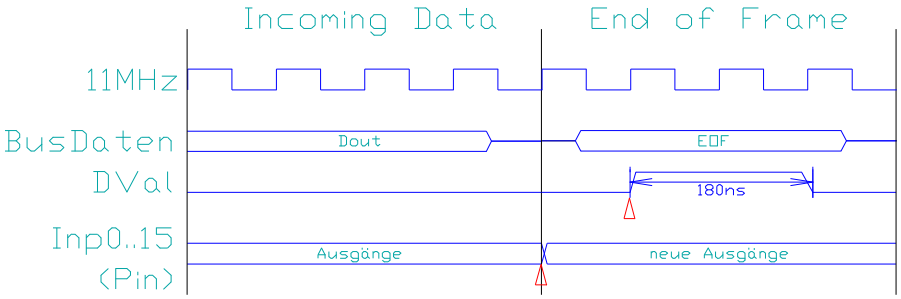
If incorrect data is received (interference), the last value correctly received will be retained.
With Link Down, all outputs drop off .

Timing Diagram

TTL interface: Timing inputs

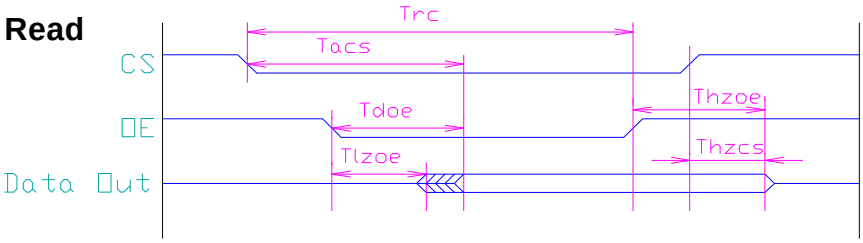


TTL interface: Timing outputs

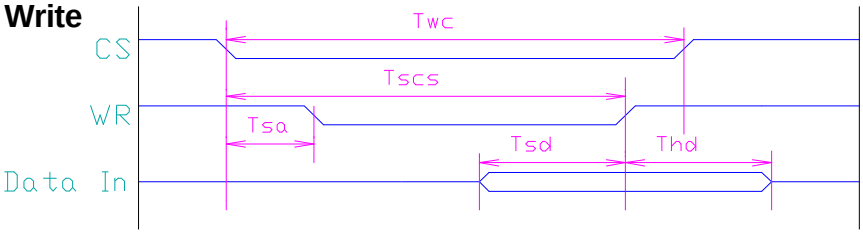


Timing Diagramm

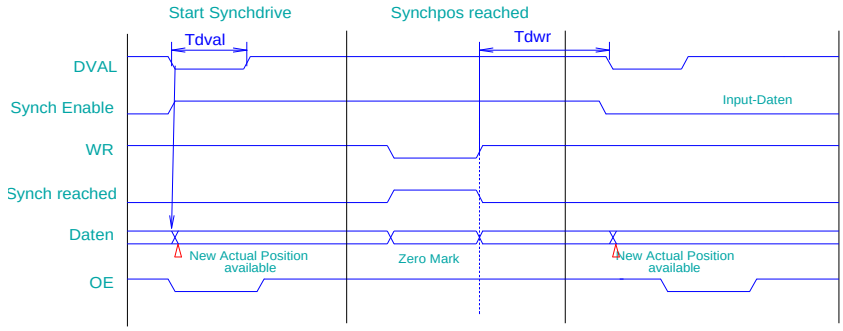
Read



Write



Timing Diagram



Read Cycle		Min	Max	Unit
Trc	Read Cycle Time	50		ns
Tacs	CS low to Data Valid		10	ns
Tdoe	OE low to Data Valid		10	ns
Tlzoe	OE low to Data out Start	10		ns
Thzoe	OE high to Data Line Tri-State		10	ns
Thzcs	CS high to Data Line Tri-State		10	ns

Write Cycle		Min	Max	Unit
Twc	Write Cycle Time	50		ns
Tscs	CS low to Write End	50		ns
Tsa	Address, CS Set Up to Write Start	0		ns
Tsd	Data Set-Up to Write End	8		ns
Thd	Data Hold From Write End	0		ns
Tdwr	Data write	4		µs

Parallel Port

INFO-TTL 97242-AMK

The parallel port uses pins 2 ... 15 of connector 1 as bidirectional I/O signals. The output signals of connector 2 are not required.

Read cycles with permanently wired CS, OE = low signals are not allowed. The logic in the GAL can in this case not load any current values to the output register.
At least one of the CS, OE control lines must be raised after the Read cycle.

Between two read cycles, at least 500ns must elapse.

Between two write cycles, at least 400ns must elapse, otherwise the GAL will be unable to accept the input values.

The "Sync_reached" signal must be transferred highly synchronously with the zero position. The zero position must always be transmitted with the "Sync_reached" signal in the same telegram.

To allow the current actual data to be transmitted in the WR cycle, the time Tdwr of 4µs is needed before the signal DVAL.